REMARKS

This is in response to the Final Office Action mailed October 3, 2002. With this Amendment, claims 1 and 5 have been amended to more clearly distinguish the present invention from the cited reference. All pending claims are presented for reconsideration and allowance.

In Section 2 of the Office Action, the Examiner objected to the title of the invention as being non-descriptive of the invention. Applicant believes that the title, as amended herein, sufficiently describes the invention. Withdrawal of the objection is respectfully requested.

In Section 4 of the Office Action, the Examiner rejected claims 1, 2, 4 and 5 under 35 U.S.C. §102(e) as being anticipated by Borel (U.S. Patent No. 6,130,460). Applicant respectfully believes that the rejections can be withdrawn in light of the reasons set forth below.

The present invention is directed to a hard macro having an antenna rule violation free input/output port that prevents antenna rule violations from occurring altogether when used to form an integrated circuit. As a result, the present invention not only eliminates the need to perform checks for violations of antenna rules, but also eliminates the need to perform fixes to the hard macro design. As explained in the application, hard macros are predefined circuit components that perform a desired function and can be dropped into the circuit layout design and later interconnected using a conventional routing tool. Hard macros include such elements as processors, memory arrays, input and output interface circuits, encoders, decoders, and other types of circuit blocks.

Applicant has amended independent claim 1 to more clearly describe the hard macro as being a "predefined circuit element that is droppable into a floor plan of a circuit design." Claim 5

has been further amended to describe a method of defining the hard macro of claim 1, which then forms the predefined circuit mentioned above.

Anticipation of a claim requires a teaching of each limitation of the claim by the cited reference. See, e.g., *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)("A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."); *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)("The identical invention must be shown in as complete detail as is contained in the ... claim."). Applicant respectfully believes that neither claim 1 nor claim 5 is anticipated by Borel.

Borel is directed to a process for producing an integrated circuit, which includes designing a floor plan that is initially defined without regard to antenna rule violations. [Column 3, Lines 8-12] There is no mention of the circuit floor plan containing the hard macro having an antenna rule violation free input/output port described in claim 1 of the present invention. As a result, antenna rule violation checks must be made to determine whether any such violations exist. [Id.] Borel then teaches a method of fixing the violations, once discovered, substantially in the manner discussed in the background of the present application.

The Examiner submits that Borel teaches all of the elements of claims 1 and 5. In particular, the Examiner found Borel to teach the "input/output (I/O) port" as the EMP point at column 6, lines 3-12; the "top level metallic conductor of a highest level metalization layer that is electrically coupled to a diffusion region" at column 5, lines 63-67; and the "electrical connection" at column 5, lines 30-34. As pointed out by Applicant in the Amendment that was filed in response to the Office Action

mailed July 18, 2002, Applicant believes that the cited passages and elements of Borel are unrelated to the hard macro of claim 1 and the method of claim 5. In general, the cited elements and passages relate to a circuit design that requires modification, or has been modified to fix antenna rule violations, as opposed to a hard macro having an antenna rule violation free input/output port and is a "predefined circuit element that is droppable into a floor plan of a circuit design." If Borel taught such a hard macro or a method of defining such a hard macro, the method described in Borel would be unnecessary to perform.

Accordingly, Applicant respectfully believes that independent claims 1 and 5, as amended, are allowable since the cited reference fails to teach all of the elements of the claims. Applicant, therefore, requests that the rejections of claims 1 and 5 be withdrawn. Applicant further requests that the rejections of claims 2 and 4 be withdrawn since they depend from allowable base claim 1.

In Section 11 of the Office Action, the Examiner rejected claim 3 under 35 U.S.C. §103(a) as being unpatentable over Borel and Applicant's admitted prior art. Applicant respectfully believes that claim 3 is allowable since it depends from claim 1, which is believed to be allowable for the reasons set forth above. Applicant, therefore, requests that the rejection be withdrawn.

In view of the above comments and remarks, it is believed that the present application is in condition for allowance. Consideration and favorable action is respectfully requested.

The Director is authorized to charge any fee deficiency required by this paper or credit any overpayment to Deposit Account No. 23-1123.

Respectfully submitted,

WESTMAN, CHAMPLIN & KELLY, P.A.

By: _____

Brian D. Kaul, Reg. No. 41,885
Suite 1600 - International Centre
900 Second Avenue South
Minneapolis, Minnesota 55402-3319
Phone: (612) 334-3222 Fax: (612) 339-3312

BDK/djb

MARKED-UP VERSION OF REPLACEMENT PARAGRAPHS

Replacement title for the title on Page 1, line 1 and the title located in the Abstract on Page 13, line 1:

HARD MACRO HAVING AN ~~IMPROVED PORT ROUTING FOR AVOIDANCE OF~~ ANTENNA RULE VIOLATION~~S~~ FREE INPUT/OUTPUT PORTS

MARKED-UP VERSION OF REPLACEMENT CLAIMS

1. (Twice Amended) A hard macro having an antenna rule violation free input/output port~~for use in an Application Specific Integrated Circuit (ASIC)~~, comprising:

an input/output (I/O) port having a port level metallic conductor in a low level metalization layer;

an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;

a top level metallic conductor of a highest level metalization layer that is electrically coupled to a diffusion region; and

an electrical connection between the port level metallic conductor and the gate conductor including a first conducting section extending from the gate conductor to the top level metallic conductor and a second conducting section extending from the top level metallic conductor to the port level conductor~~;~~

wherein the I/O port is free of antenna rule violations, and the I/O port, the I/O transmitter, the top level metallic conductor, and the electrical connection form a predefined circuit element that is droppable into a floor plan of a circuit design.

5. (Amended) A method of defining~~forming~~ a hard macro having an antenna rule violation free input/output port~~for use in an Application Specific Integrated Circuit~~, comprising steps of:

~~(a)~~(f) ~~forming~~defining an input/output (I/O) port having a port level conductor ~~of the I/O port~~ in a low level metalization layer;

~~(b)~~(g) ~~forming~~defining an I/O transistor having a gate conductor separated from a diffusion region by a gate oxide layer;

~~(c)~~(h) ~~forming~~defining a top level metallic conductor in a highest level metalization layer that is electrically coupled to a diffusion region;

~~(d)~~(i) ~~forming~~defining a first conducting section of an electrical connection extending from the gate conductor to the top level metallic conductor; and

~~(e)~~(j) ~~forming~~defining a second conducting section of the electrical connection extending from the top level metallic conductor to the port level conductor;~~.~~

wherein the defined I/O port is free of antenna rule violations, and the defined I/O port, transistor, top level metallic conductor, and electrical connection form a predefined circuit element that is droppable into a floor plan of a circuit design.